UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/556,647	11/10/2005	Michael Robbe	28944/40163	6584

29471 7590 08/07/2008
MCCRACKEN & FRANK LLP
311 S. WACKER DRIVE
SUITE 2500
CHICAGO, IL 60606

EXAMINER	
ALMO, KHAREEM E	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
08/07/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/556,647	ROBBE ET AL.	
	Examiner	Art Unit	
	KHAREEM E. ALMO	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-13* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 7 and 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan (US 6693494) in view of (Nilson and Riedel, Electric Circuits fifth edition figure 6.17 pg 227)

3. With respect to claim 1, figures 6, 4 and 3 of Fan (US 6693494) discloses a voltage shift control circuit intended to be placed in parallel with at least one voltage shift capacitor (C1) coupling the phase comparator (21) and the voltage controlled oscillator (23) of a phase locked loop, and comprising: an input (input to the charge pump A), intended to be coupled with the output of the phase comparator; an output (output of the loop filter 22), intended to be coupled with the input of the voltage controlled oscillator; controlled charging means (FIG 6), designed to charge the voltage shift capacitor (C3) according to a control signal (NORMAL MODE, SPEEDUP MODE OR PRECHARGE MODE); controlled pre-charging means (62, 63, 64, 65, Sb and Sc), designed to accelerate (via SPEEDUP MODE) the charging of the voltage shift capacitor by the controlled charging means; and controlled polarization means (40 of figure 4), designed to ensure the polarization of the input during the pre-charging of the

voltage shift capacitor but fails to disclose at least one series voltage shift capacitor. Figure 6.17 of Riedel teaches the use of 3 series capacitors to replace one capacitor. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a number of capacitors in series for one a larger equivalent capacitor for the well known purpose of optimizing the value of the capacitance.

With respect to claim 7, the above combination discloses the circuit according to Claim 1, further comprising means (Sc) for deactivating the controlled pre-charging means before the controlled polarization means.

With respect to claim 10, the above combination discloses the circuit according to claim 1, designed in CMOS technology (Note this claim is deemed obvious expedient to one skilled in the art to design the circuit using CMOS technology).

With respect to claim 11, the combination above discloses the Phase locked loop comprising a phase or frequency comparator (21), a loop filter (22), a voltage controlled oscillator (23), a voltage shift capacitor (C3) connecting the phase comparator and the voltage controlled oscillator, and a voltage shift control circuit according to Claim 1 placed in parallel with the voltage shift capacitor (C3) and comprising : an input, intended to be coupled with the output of the phase comparator; an output, intended to be coupled with the input of the voltage controlled oscillator (23); controlled charging means (60, 61), designed to charge the voltage shift capacitor according to a control signal; controlled pre-charging means(62, 63, 64, 65, Sb and Sc), designed to accelerate the charging of the voltage shift capacitor by the controlled charging means;

and controlled polarization means (40), designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor but fails to disclose a series voltage shift capacitor. Figure 6.17 of Riedel teaches the use of 3 series capacitors to replace one capacitor. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a number of capacitors in series for one a larger equivalent capacitor for the well known purpose of optimizing the value of the capacitance.

With respect to claim 12, the combination above discloses the Radio-frequency transmitter (Note: the recitation of the Radio frequency transmitter is deemed intended use because the circuit of claim 1 can be put into a variety of circuits), phase locked loop generating a radio-frequency signal to be transmitted, said phase locked loop comprising a phase or frequency comparator, a loop filter, a voltage controlled oscillator, a Voltage shift capacitor connecting the phase comparator and the voltage controlled oscillator, and a voltage shift control circuit according to Claim 1 placed in parallel with the voltage shift capacitor and comprising: an input, intended to be coupled with the output of the phase comparator; an output, intended to be coupled with the input of the voltage controlled oscillator; controlled charging means (60, 61), designed to charge the voltage shift capacitor according to a control signal; controlled pre-charring means (62, 63, 64, 65, Sb and Sc), designed to accelerate the charging of the voltage shift capacitor by the controlled charging means; and controlled polarization means (40), designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor.

With respect to claim 13, the combination above discloses the Mobile terminal of a radio-communications system with a radio-frequency transmitter (Note: the recitation of the Radio frequency transmitter and the Mobile terminal is deemed intended use because the circuit of claim 1 can be put into a variety of circuits), having a phase locked loop for generating a radio-frequency signal to be transmitted, said phase locked loop comprising a phase or frequency comparator, a loop filter, a voltage controlled oscillator, a voltage shift capacitor connecting the phase comparator and the voltage controlled oscillator, and a voltage shift control circuit according to Claim 1 placed in parallel with the voltage shift capacitor and comprising: an input, intended to be coupled with the output of the phase comparator; an output, intended to be coupled with the input of the voltage controlled oscillator; controlled charging means, designed to charge the voltage shift capacitor according to a control signal; controlled pre-charging means, designed to accelerate the charging of the voltage shift capacitor by the controlled charging means; and controlled polarization means, designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor.

With respect to claim 14, the combination above discloses the Base station of a radio-communications system with a radio-frequency transmitter (Note: the recitation of the Radio frequency transmitter and the Base station is deemed intended use because the circuit of claim 1 can be put into a variety of circuits), having a phase locked loop for generating a radio-frequency signal to be transmitted, said phase locked loop comprising a phase or frequency comparator, a loop filter, a voltage controlled oscillator, a voltage shift capacitor connecting the phase comparator and the voltage

controlled oscillator, and a voltage shift control circuit according to Claim 1 placed in parallel with the voltage shift capacitor and comprising: an input, intended to be coupled with the output of the phase comparator; an output, intended to be coupled with the input of the voltage controlled oscillator; controlled charring means, designed to charge the voltage shift capacitor according to a control signal; controlled pre-charging means, designed to accelerate the charging of the voltage shift capacitor by the controlled charging means; and controlled polarization means, designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor.

4. Claims 2-5, 8 and 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Fan (US 6693494) in view of Kumar et al. (US 6611161) in further view of of (Nilson and Riedel, Electric Circuits fifth edition figure 6.17 pg 227)

With respect to claim 2, figures 6, 4 and 3 of Fan (US 6693494) discloses a voltage shift control circuit intended to be placed in parallel with at least one voltage shift capacitor (C1) coupling the phase comparator (21) and the voltage controlled oscillator (23) of a phase locked loop, and comprising: an input (input to the charge pump A), intended to be coupled with the output of the phase comparator; an output (out of 22), intended to be coupled with the input of the voltage controlled oscillator; controlled charging means (FIG 6), designed to charge the voltage shift capacitor (C3) according to a control signal (NORMAL MODE, SPEEDUP MODE OR PRECHARGE MODE); controlled pre-charging means (62, 63, 64, 65, Sb and Sc), designed to accelerate (via SPEEDUP MODE) the charging of the voltage shift capacitor by the

controlled charging means; and controlled polarization (division into two opposites) means (40 of figure 4), designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor but fails to disclose wherein the controlled charging means comprise a first operational amplifier connected as a voltage follower between the input and the output, a resistor (R3) placed in the feedback loop of the operational amplifier, and a controlled current source (60) supplying a current (at node output from 60) of specified value through said resistor and fails to disclose a series voltage shift capacitor. Figure 4 of Kumar teaches the use of a unity gain amplifier (240) at the output of the charge pump to suppress charge sharing from parasitic capacitances. It would have been obvious at the time the invention was made to use the unity gain amplifier of Kumar in the circuit of Fan for the purpose of suppressing charge sharing from parasitic capacitances. Figure 6.17 of Riedel teaches the use of 3 series capacitors to replace one capacitor. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a number of capacitors in series for one a larger equivalent capacitor for the well known purpose of optimizing the value of the capacitance.

With respect to claim 3, the combination above discloses the circuit according to Claim 2, wherein the operational amplifier of the charging means comprise a push-pull output stage (60 and 61)-and wherein the charging means further comprise a resistor (R3) of high value connected in series between the output of the operational amplifier and the output of the circuit.

With respect to claim 4, the combination above discloses the circuit according to

Claim 3, wherein the controlled pre-charging means comprise a push-pull stage (64 65) which, in the activation of the pre-charging means configuration, is arranged as a mirror with respect to the push-pull output stage of the operational amplifier of the charging means, in such a way as to short-circuit the high value resistor.

With respect to claim 5, figure discloses the circuit according to Claim 4, wherein the push-pull stage (64 and 65) of the pre-charging means (62, 63, 64, 65, Sb and Sc) is designed to deliver a current higher than the current delivered by the push-pull output stage of the operational amplifier of the charging means.

With respect to claim 8, the combination above discloses circuit according to Claim 2 further comprising an additional controlled push-pull stage (62 and 63) whose output is intended to be connected to the centre point of an RC network of a loop filter (22) of the PLL and which, in the activation configuration, is connected as a mirror with respect to the push-pull stage (64 and 65) of the controlled pre-charging (62, 63, 64, 65, Sb and Sc) means and with respect to the push-pull output stage of the operational amplifier of the charging means.

With respect to claim 9, the combination above discloses circuit according to Claim 8, wherein the additional controlled push-pull stage (62 and 63) is integrated with the operational amplifier of the charging means.

Allowable Subject Matter

5. Claim 6 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 6, the prior art fails to disclose or suggest the circuit according to claim 1 wherein the controlled polarization means comprises a second operational amplifier connected as a voltage follower as disclosed.

Response to Arguments

6. Applicant's arguments with respect to claim 1-13 have been considered but are moot in view of the new ground(s) of rejection.

With respect to applicant's argument that Fan does no disclose a series capacitor, it is obvious to use one or more capacitors to derive an equivalent capacitance as disclosed in the new rejection above. It is the examiners view that this combination would result in the invention disclosed by the applicant.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/K. E. A./
Examiner, Art Unit 2816

/QUAN TRA/
Primary Examiner, Art Unit 2816